Code.No: 07A51101 | R07 | SET-1

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
DIGITAL SIGNAL PROCESSING
(COMMON TO BME, E.COMP.E)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1.a) Verify whether the following systems are linear and time invariant or not
i) $y(n) = a(n)x(n)$ ii) $y(n) = ax(n-1) + bx(n-2)$
b) The discrete time systems are represented by the difference equations in which x(n) is the input and y(n) is the output given by $y(n) = x(n+1)-3x(n)+x(n-1)$; $n \geq 0$. Check whether the system defined above is linear, time invariant and causal or not. [8+8]

2.a) Define DFT and IDFT. Compute the DFT of the given time domain sequence $x(n) = \{1,2,3,4,4,3,2,1\}$.
b) List out the properties of DFT with necessary expressions. [8+8]

3. Compute FFT of the given sequence $x(n) = \{8, 3, 5, 6, 7, 8, 4, 5\}$ using Radix-2 DIT FFT Algorithm and verify using IFFT-DIT Algorithm. [16]

4.a) Define Z- Transform. Determine the impulse response for the systems given by the difference equation $y(n) = x(n)+3x(n-1)-4x(n-2)+2x(n-3)$
b) Obtain the Parallel and Cascade form realization of the given LTI system governed by the difference equation $y(n) = -3/8\ y(n-1) + 3/32\ y(n-2) + 1/64\ y(n-3) + x(n) + 3\ x(n-1) + 2\ x(n-2)$. [8+8]

5.a) Compare and Contrast Bilinear & Impulse Invariant transformation technique
b) Design a Digital Butterworth LPF using Bilinear transformation technique for the following specifications

$$0.707 \leq |H(w)| \leq 1 \quad ; 0 \leq w \leq 0.2\pi$$
$$|H(w)| \leq 0.08 \ ; 0.4\pi \leq w \leq \pi$$

[8+8]

6.a) Compare various windowing techniques w.r.t sidelobes and beamwidth
b) Design an FIR Digital High pass filter using Hamming window whose cutoff freq is 1.2 rad/s and length of window N=9. [8+8]

7.a) What is the importance of Multirate Signal Processing and hence define Decimation and Interpolation.
b) Discuss the process of decimation with a neat block diagram and explain how the aliasing effect can be avoided. [8+8]

8.a) Discuss the internal architecture of a TMS 320C54xx Digital signal processor
b) Explain six stage pipeline architecture of TMS320C54xx processor. [8+8]

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Code.No: 07A51101 | R07 | SET-2

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
DIGITAL SIGNAL PROCESSING
(COMMON TO BME, E.COMP.E)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1.a) Define Linearity, Time invariant, Stability and Causality
b) A second order discrete time system is characterized by the difference equation y(n)-0.1y(n-1)-0.02y(n-2)=2 x(n)-x(n-1). Determine y(n) for n≥0 when x(n) = u(n) and the initial conditions are y(-1)= 10 and y(-2) = 5. [8+8]

2.a) Define DFT and IDFT. Compute the IDFT of the given time domain sequence x(n) = { 1,2,3,4,4,3,2,1}.
b) Bring out the relationship between DFT and Z- Transform. [8+8]

3. Derive the necessary expressions for computing FFT using DIF Algorithm and hence Compute FFT of the given sequence x(n) = {1,2,3,4,4,3,2,1} using Radix-2 DIF FFT Algorithm. [16]

4.a) Define Z- Transform. Determine the impulse response for the systems given by the difference equation y(n) +3y(n-1)+2y(n-2) = 2x(n)-x(n-1)
b) Obtain the Direct Form - I and Direct form - II realization of the given LTI system governed by the difference equation
y(n) = - 3/8 y(n-1) + 3/32 y(n-2) + 1/64 y(n-3) + x(n) + 3 x(n-1) + 2 x(n-2). [8+8]

5.a) Compare and Contrast Butterworth and Chebyshev approximations.
b) Compute the poles of an Analog Chebyshev filter TF that satisfies the Constraints
$0.707 \le |H(j\Omega)| \le 1 \quad ; 0 \le \Omega \le 2$
$|H(j\Omega)| \le 0.1 \; ; \Omega \ge 4$
and determine Ha(s) and hence obtain H(z) using optimum transformation. [8+8]

6.a) Show that FIR filters exhibit linear phase.
b) Design a High Pass FIR filter whose cut-off frequency is 1.2 radians/sec and N = 9 using Hamming Window and draw the frequency response curve. [8+8]

7.a) Discuss the process of Interpolation with a neat block diagram.
b) Explain the implementation of polyphase filter structure for interpolators. [8+8]

8.a) Discuss various data addressing modes of TMS320C54xx processors
b) Explain six stage pipeline architecture of TMS320C54xx processor. [8+8]

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Code.No: 07A51101 | R07 | SET-3

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
DIGITAL SIGNAL PROCESSING
(COMMON TO BME, E.COMP.E)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1.a) Discuss various discrete time sequences.
b) Find the frequency response of the LTI system, governed by the difference equation x(n) = y(n) – 2y(n-1)-4y(n-2). [8+8]

2.a) Find X(K) of the given time domain sequence x(n) = {1,2,3,4,5,6,7,8}.
b) Define DFS and list out its properties. [8+8]

3. Develop DIF FFT algorithm for decomposing the DFT for N=12 by considering the factors N = 3.4 and compute for x(n) = {1,2,3,4,5,6} [16]

4.a) What are the basic blocks of filter realization structures? Hence discuss Cascade and Parallel form of realization of structures.
b) Obtain the cascade and parallel realization structures for the following signal
y(n) = ¾ y(n-1) – 1/8 y(n-2) + x(n) + 1/3 x(n-1). [8+8]

5.a) Compute the poles of an Analog Chebyshev filter TF that satisfies the Constraints
$0.707 \leq |H(j\Omega)| \leq 1 \; ; 0 \leq \Omega \leq 2$
$|H(j\Omega)| \leq 0.1 \; ; \Omega \geq 4$
and determine Ha(s) and hence obtain H(z) using Optimum transformation.
b) Discuss the frequency warping effect in realization of digital filters using Bilinear transformation method. [8+8]

6.a) Compare FIR and IIR filters
b) Design a bandstop filter to reject frequencies in the range 1 to 2 rad/s using Hamming window with N=7. [8+8]

7. a) Discuss the Process of decimation with the help of necessary equations
b) Discuss in brief about polyphase realization of Interpolators. [8+8]

8. a) Explain six stage pipeline architecture of TMS320C54xx processor.
b) Discuss various data addressing modes of TMS320C54xx processors. [8+8]

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Code.No: 07A51101 | R07 | SET-4

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
DIGITAL SIGNAL PROCESSING
(COMMON TO BME, E.COMP.E)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1.a) Check whether the following systems are linear and time invariant
i) $y(n) = n.(x(n))^2$ ii) $y(n) = a(x(n))^2 + bx(n)$
b) Obtain the necessary and sufficient condition for BIBO stability. [8+8]

2.a) What is the importance of DFT and hence bring out the relation between Z-Transform and DFT.
b) Compute the convolution of two given sequences x(n) = {1 2 3 4} and y(n) = {4 3 2 1}using DFT. [8+8]

3.a) Compare the Computational complexity of DFT and FFT.
b) Develop DIT FFT algorithms for decomposing the DFT for N=6 and draw the flow diagrams for N = 2, 3 and apply for the computation of DFT for x(n) = {1,2,3,4,5,6} [8+8]

4.a) Define Z- Transform and List out the properties of Z- Transform.
b) Determine the parallel realizations of IIR digital filter transfer function:
$H(Z) = 3 (Z^2+5Z+4) / (2Z+1)(Z+2)$ [8+8]

5.a) Explain the aliasing effect in realization of digital filters using Impulse invariant technique.
b) Convert the analog filter into a digital filter whose system function is
$H(S) = (S+0.2) / (S+0.2)^2 + 9$ using impulse invariant technique. Assume T =0.5s [8+8]

6.a) Compare FIR and IIR filters.
b) Design a bandpass filter to pass frequencies in the range 1 to 2 rad/s using Hamming window with N=5. [8+8]

7.a) Define Decimation and Interpolation.
b) Discuss the sampling rate conversion by a factor I/D with necessary equations. [8+8]

8.a) Discuss the internal architecture of a TMS 320C54xx Digital signal processor.
b) Discuss various data addressing modes of TMS320C54xx processors. [8+8]

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